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Title:

OFF-CHIP DRIVER CIRCUIT AND DATA OUTPUT CIRCUIT USING THE SAME

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BACKGROUND

1. Field of the Invention

[0001] The present invention relates to a semiconductor device and, more particularly, to an off-chip driver circuit and an output circuit using the same.

2. Discussion of Related Art

[0002] In designing integrated circuits (ICs) such as a memory chip, an off-chip driver circuit is used to transfer data information from the memory chip to external environments. In general, the off-chip driver circuit functions to transfer an internal data signal of a chip to external system environments at possible high speed.

[0003] A data output circuit having an off-chip driver circuit according to a prior art will be described with reference to Fig. 1, which shows a block diagram schematically illustrating the configuration of a data output circuit 10 having an off-chip driver circuit in a related art.

[0004] The off-chip driver circuit 100 includes off-chip drivers 100-1 to 100-N. Each of the off-chip drivers 100-1 to 100-N uses the same data signal as one input and corresponding first to N^{th} control signals (N is a natural number of 2 or more) as the other input. Each of the off-chip drivers 100-1 to

100-N functions to reflect a possible difference in the performance of a device according to process conditions performed. Furthermore, each of the off-chip drivers is connected correspondingly to output driver within an output driver circuit 300. If a corresponding off-chip driver is turned off, an output driver connected thereto is turned off, and if a corresponding off-chip driver is turned on, an output driver connected thereto is turned on.

[0005] If an off-chip driver circuit operates in a high frequency state, however, data signals outputted from the off-chip driver circuit are turned on/off at the same time. It is therefore not technically easy to make an output (Dout) waveform of the output driver circuit 300 having an adequate slew. For example, in products such as a double data rate (DDR), etc. for implementing an ultrahigh speed operation, slew of an output waveform may become great and overshoot may thus take place. This causes the properties of a system interface to be significantly degraded.

SUMMARY OF THE INVENTION

[0006] The present invention is directed to provide an output waveform having an adequate slew.

[0007] The present invention relates to an off-chip driver circuit that can distribute On/Off time points of an off-chip driver into adequate time intervals.

[0008] The present invention is concerned with an off-chip driver circuit and data output circuit using the same, which can enhance the properties of a system interface.

[0009] According to one preferred embodiment of the present invention, there is provided an off-chip driver circuit having first to N^{th} off-chip drivers for using a data signal and first to N^{th} control signals respectively to determine whether to produce output signals according to corresponding control signals, being characterized in that at least one of the first to N^{th} off-chip drivers includes a delay circuit(s) for outputting a signal having a given delay time compared with other signals of the remaining off-chip drivers.

[0010] Meanwhile, the delay circuit can be added to an input terminal or an output terminal of the off-chip driver. Each of the off-chip drivers may be constructed to perform an NAND operation for a corresponding control signal and the data signal when a logical status of the inputted data signal is High, and an NOR operation for an inverse signal of a corresponding control signal and the data signal when a logical status of the inputted data signal is Low.

[0011] Furthermore, each of the off-chip drivers is connected to the corresponding output driver, and if a control signal of a given off-chip driver is at an enable level, an output driver connected to the given off-chip driver is driven.

[0012] According to another preferred embodiment of the present invention, there is provided a data output circuit, including an off-chip driver circuit having first to N^{th} off-chip drivers for using a data signal and first to N^{th} control signals respectively to determine whether to produce output signals according to corresponding control signals, a pre-driver circuit for using the data signal to drive an output driver circuit, and the output driver circuit

connected to the outputs of the off-chip driver circuit and the pre-driver circuit, wherein at least one of the first to N^{th} off-chip drivers includes a delay circuit(s) for outputting a signal having a given delay time compared with other signals of the remaining off-chip drivers.

[0013] In the above, the pre-driver circuit may be constructed to receive the data signal and pulls up or pulls down according to a logical status of the data signal. The output driver circuit includes each of the output drivers corresponding to the off-chip drivers, wherein if a control signal of a given off-chip driver is at an enable level, an output driver connected to the given off-chip driver may be driven.

BRIEF DESCRIPTION OF THE DRAWINGS

[0014] Fig. 1 is a block diagram schematically illustrating the configuration of a data output circuit including an off-chip driver circuit in a related art;

[0015] Fig. 2 is a block diagram schematically illustrating the configuration of a data output circuit having an off-chip driver circuit according to an embodiment of the present invention;

[0016] Fig. 3 shows an exemplary configuration of an off-chip driver circuit that operates when a logical High data signal is applied in the data output circuit according to an embodiment of the present invention;

[0017] Fig. 4 shows an exemplary configuration of an off-chip driver circuit that operates when a logical Low data signal is applied in the data output circuit according to an embodiment of the present invention;

[0018] Fig. 5 shows an exemplary configuration of a delay circuit that is applied to the off-chip driver circuit according to an embodiment of the present invention;

[0019] Fig. 6 shows an exemplary configuration of a pre-driver circuit in the data output circuit according to an embodiment of the present invention;

[0020] Fig. 7 is a conceptual view for explaining that signals outputted from the off-chip drivers have given delay times according to an embodiment of the present invention; and

[0021] Fig. 8 is a graph showing results of comparing a waveform of a signal outputted from the output driver circuit, where the off-chip driver according to an embodiment of the present invention is applied, with a waveform of a signal in a related art.

DETAILED DESCRIPTION OF PREFERRED EMBODIMENTS

[0022] Now the preferred embodiments according to the present invention will be described with reference to the accompanying drawings. Since preferred embodiments are provided for the purpose that the ordinary skilled in the art are able to understand the present invention, they may be modified in various manners and the scope of the present invention is not limited by the preferred embodiments described later.

[0023] Fig. 2 is a block diagram schematically illustrating the configuration of a data output circuit including an off-chip driver circuit according to an embodiment of the present invention.

[0024] A data output circuit 1 shown in Fig. 2 includes an off-chip driver circuit 100 having first to Nth delay circuits 100b; 110-1 to 110-N and first to Nth off-chip drivers 100a; 100-1 to 100-N, a pre-driver circuit 200, and an output driver circuit 300 connected to output signals of the off-chip driver circuit 100 and the pre-driver circuit 200. In the above, N is a natural number of 2 or more.

[0025] The off-chip driver circuit 100 includes the first to Nth off-chip drivers 100-1 to 100-N. Each off-chip driver receives a data signal (DATA) and a corresponding control signal to determine whether to produce an output signal according to the corresponding control signal. The control signal checks a wafer status, after a process is performed, and determines On/Off statuses of each off-chip driver based on the check result. The first to Nth control signals are constructed accordingly. For instance, if a single off-chip driver is constructed to have the drivability of 10% and the pre-driver circuit 200 is constructed to have the drivability of 60%, eight off-chip drivers can be constructed to exhibit a total drivability of 60% to 140%, which can be varied in a distance of 10%. For instance, if a single off-chip driver is desired to have a total drivability of 80%, the drivability of 20% is further needed in addition to the 60% drivability of the pre-driver circuit 200. Two of the eight off-chip drivers constituting the off-chip driver circuit 100 are turned on.

[0026] Therefore, it is determined whether each of the off-chip drivers 100-1 to 100-N has to be turned on/off by calibrating the off-chip drivers 100-1 to 100-N from an impedance matching viewpoint for a memory chip of a system. It is thus possible to determine the drivability of the output driver

circuit 300 driven by the off-chip drivers 100-1 to 100-N. Whether each off-chip driver must be turned on/off can be controlled by a corresponding control signal. A wafer status is checked and whether each off-chip driver must be turned on/off is then determined based on the check result. The first to N^{th} control signals can be constructed accordingly. The first to N^{th} control signals can be inputted from a chip set (now shown).

[0027] Furthermore, at least one of the first to N^{th} off-chip drivers 100-1 to 100-N in the off-chip driver circuit 100 has a delay circuit for outputting a signal having a given delay time compared with output signals of the remaining off-chip drivers. For example, if the off-chip driver circuit 100 consists of two off-chip drivers, there is a delay time between two output signals from the off-chip driver.

[0028] The delay circuit that can be connected to each of the off-chip drivers may be constructed to delay the data signal (DATA) with the delay circuit added to the input terminal of the off-chip driver, or may be constructed to delay the output signal outputted from the off-chip driver with it added to the output terminal of the off-chip driver.

[0029] The pre-driver circuit 200 uses the data signal (DATA) received thereto to perform a pull up or pull down function depending on a logical status of the data signal. Meanwhile, the pre-driver circuit 200 is connected to a corresponding output driver of the output driver circuit 300 and drives the output driver.

[0030] The output driver circuit 300 may have output drivers each corresponding to the off-chip drivers of the off-chip driver circuit 100. If a

control signal of a given off-chip driver is at an enable level (for example, a logical High), the output driver circuit 300 drives an output driver connected to the given off-chip driver.

[0031] Detailed configurations of the off-chip driver circuit, the pre-driver circuit, and the output driver circuit will now be described.

[0032] Fig. 3 shows an exemplary configuration of an off-chip driver circuit that operates when a logical High data signal is applied in the data output circuit according to an embodiment of the present invention, and Fig. 4 shows an exemplary configuration of an off-chip driver circuit that operates when a logical Low data signal is applied in the data output circuit according to an embodiment of the present invention.

[0033] Referring to Fig. 3, each of the off-chip drivers 100-1 to 100-N in the off-chip driver circuit 100 includes two inverters INV11 and INV12 to INVN1 and INVN2 for using the control signals (first to N^{th} control signals) to output twice-inverted signals, and NAND devices NAND11 to NANDN1 for using the twice-inverted signals and the data signal (DATA) to perform an NAND operation. For example, in order to turn on a corresponding off-chip driver, a corresponding control signal may be inputted as a logical High. In order to turn off a corresponding off-chip driver, a corresponding control signal may be inputted as a logical Low.

[0034] The operation of each of the off-chip drivers 100-1 to 100-N will be described as follows. If the data signal (DATA) is inputted as a logical High, the same logical High is inputted to one terminal of each of the off-chip drivers 100-1 to 100-N. Therefore, if a control signal inputted to the other

terminal thereof is inputted as a logical High, a signal outputted from an NAND device becomes a logical Low. If a control signal inputted to the other terminal is inputted as a logical Low, a signal outputted from the NAND device becomes a logical High. These output signals (OUT1 to OUTN) are inputted to the output driver circuit 300. Regarding an output driver circuit 300a, it is to be noted that a portion of the output driver circuit connected to the pre-driver circuit 200 is omitted from the drawing, but only a portion of the output driver circuit 300 connected to the off-chip driver is shown. In case where the output signal is logically Low, a PMOS transistor of the output driver circuit connected thereto is driven.

[0035] Delay circuits 110-1 to 110-N are added to respective input terminals of the off-chip drivers 100-1 to 100-N shown in Fig. 3, so that at least two of the input signals (DATA) transferred to the off-chip drivers have different delay times. For example, the delay time may be set to 50 to 300ps. As another variant, the delay circuits 110-1 to 110-N may be added to the respective output terminals OUT1 to OUTN of the off-chip driver.

[0036] Referring to Fig. 4, each of the off-chip drivers 100-1 to 100-N in the off-chip driver circuit 200 includes inverters INV11 to INVN1 for using control signals (first to Nth control signals) to output inverted signals, and NOR devices NOR11 to NORN1 for using the inverted signals and the data signals (DATA) to perform an NOR operation. In order to turn on a corresponding off-chip driver, a corresponding control signal may be inputted as a logical High. In order to turn off a corresponding off-chip driver, a corresponding control signal may be inputted as a logical Low.

[0037] The operation of each of the off-chip drivers 100-1 to 100-N will be described as follows. If the data signal (DATA) is inputted as a logical Low, the data signal (DATA) of the logical Low is inputted to one terminal of each of the off-chip drivers 100-1 to 100-N. If a control signal inputted to the other terminal thereof is inputted as a logical High, a signal outputted from a corresponding NOR device becomes a logical High. If a control signal inputted to the other terminal thereof is inputted as a logical Low, a signal outputted from the NAND device becomes a logical High. These output signals (OUT1 to OUTN) are inputted to the output driver circuit 300. With respect to the output driver circuit having a reference numeral 300, it is to be noted that a portion of the output driver circuit connected to the pre-driver circuit is omitted, but only a portion of the output driver circuit 300 connected to the off-chip driver is shown. In case where the output signal becomes a logical High, an NMOS transistor of the output driver circuit connected thereto is driven.

[0038] In applying the above-mentioned off-chip driver circuit to the actual world, it may be constructed so that the off-chip driver circuit and the output driver circuit shown in Fig. 3 are driven when a data signal of a logical High is applied and so that the off-chip driver circuit and the output driver circuit shown in Fig. 4 are driven when the data signal is logically Low. Furthermore, the above-mentioned off-chip driver circuit may be constructed so that the output signal is delayed only when the data signal of a logical High is applied or the data signal of a logical Low is applied.

[0039] Fig. 5 shows an exemplary configuration of the delay circuits. The delay circuits in Fig. 5 may be constructed so that signals outputted via them have different delay times through control of resistors such as R11, R12, R21, R22, etc. Another delay circuit may be constructed by serially connecting two inverters. For example, the number of an inverter serially connected to each off-chip driver has even numbers such as 2, 4, 6, etc. so that each off-chip driver has a different delay time.

[0040] Fig. 6 shows an exemplary configuration of the pre-driver circuit 200 in the data output circuit according to an embodiment of the present invention. The pre-driver circuit 200 has a pull-up unit 200a and a pull-down unit 200b in order to perform a pull-up or pull-down function depending on a logical status. The pull-up unit 200a consists of first to N^{th} PMOS 1P to NP and the pull-down unit 200b consists of first to N^{th} NMOS 1N to NN. Therefore, if the data input signal (DATA) is logically High, the output of the pre-driver circuit 200 becomes a logical Low by the pull-down unit 200b. If the data input signal (DATA) is logically Low, the output of the pre-driver circuit 200 becomes a logical High by the pull-up unit 200a. It is shown in Fig. 6 that the pre-driver circuit 200 has one pre-driver (having one pull-up unit and one pull-down unit). It is, however, should be noted that the pre-driver circuit 200 may be constructed to have two or more pre-drivers. In this case, the size of each of the pre-drivers may be different.

[0041] The operation of the off-chip driver circuit according to an embodiment of the present invention will be described in detail with reference to Fig. 2, Fig. 7 and Fig. 8.

[0042] The data signal (DATA) of a logical High or a logical Low is inputted to the off-chip driver circuit 100 and the pre-driver circuit 200. The data signal (DATA) inputted to the pre-driver circuit 200 drives the output driver circuit 300. The data signal (DATA) inputted to the off-chip driver circuit 100 allows the delay circuits added to the respective off-chip drivers to have different delay times. Such a delay time allows the time when a driving device (for example, a MOS device) of the output driver circuit 300 is turned on to have a given time difference. Fig. 7 is a conceptual view for explaining that signals (OUT1 to OUTN) outputted from the off-chip drivers are varied with given delay times (△1, △2...).

[0043] Fig. 8 is a graph showing results of comparing a waveform of a signal outputted from the output driver circuit 300 where the off-chip driver according to an embodiment of the present invention is applied, and a waveform of a signal in a related art. As can be seen from Fig. 8, in the output waveform of a related art, overshoot (V) occurs due to excessive slew. On the contrary, in the waveform of the present invention, overshoot rarely happens. Furthermore, in the present invention, the output driver circuit 300 can be controlled so that the output signal has an adequate slew.

[0044] According to the present invention described above, a data output circuit can be constructed so that an output signal has an adequate slew. In particular, in products such as a semiconductor memory for implementing an ultrahigh speed operation, i.e., DDR, etc., slew of an output waveform can be controlled. Therefore, the present invention has an effect that it can enhance properties of a system interface.

[0045] Although the foregoing description has been made with reference to the preferred embodiments, it is to be understood that changes and modifications of the present invention may be made by the ordinary skilled in the art without departing from the spirit and scope of the present invention and appended claims.